# LOYOLA COLLEGE (AUTONOMOUS), CHENNAI - 600034 

U.G. DEGREE EXAMINATION - ALLIED OPTIONAL

THIRD SEMESTER - APRIL 2022
UPH 3405 - DIGITAL ELECTRONICS

Date: 21-06-2022 $\square$ Max. : 100 Marks
Time: 01:00 PM - 04:00 PM

## PART - A

Q. No Answer ALL Questions
( $10 \times 2=20$ Marks)
1 Draw the logic symbol of T flip flop and give its truth table.
2 Find the complement of AD+BC
3 Simplify using K-map $=\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C})=\Sigma(0,2,4,6,7)$
4 Add 14 and 4 using binary addition.
5 Convert binary number (1101) 2 to hexadecimal number.
6 Draw the circuit diagram of a three-bit ring counter.
7 What is meant by a shift register?
8 Differentiate between synchronous and asynchronous counters.
9 What is meant by product of sum method?
10 Draw the circuit of a RS flip flop and give its truth table.

> PART - B

Answer any FOUR Questions
(4 x $7.5=30$ Marks)
11 Simply using K map $Y=F(A, B, C, D)=\Sigma(0,2,34,6,8,9,11,13,14,16)$
12 a) Explain shift right shift register with a neat diagram.
b) Convert the following hexadecimal to decimal (D4) н and (325) н

13 With a neat circuit, explain the working of a JK flip flop and give its truth table.
14 Discuss quads and octets in K map with an example each.
15 With a neat circuit, explain the working of a clocked RS flip flop and give its truth table.
16 Explain in detail the working of a synchronous up counter.

## PART - C

Answer any FOUR Questions
( $4 \times 12.5=50$ Marks $)$
17 a) Differentiate between minterm and maxterm.
b) Explain in detail how NAND and NOR can be used as universal gates.

18 Explain with a neat logic diagram the working of serial-in serial- out and serial-in parallel-out shift registers.
19 a)What are counters? Discuss the working of $\bmod 4$ and $\bmod 8$ counters.
b)What is meant by positive and negative logic?

20 Discuss the operation of 3-bit ripple up counter.
21 a) Explain the working of a D-flip flop and T flip flop with its truth table.
b) Solve any three Boolean theorems.

22 a) Solve the following 4 variable $K$ map: $F(P Q R S)=\Sigma(0,2,5,7,9,10,12,14)$
b) What is meant by NAND latch?

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