LOYOLA COLLEGE (AUTONOMOUS), CHENNAI – 600 034

B.Sc. DEGREE EXAMINATION – **COMPUTER SCIENCE**

THIRD SEMESTER – NOVEMBER 2011

PH 3106/CS 3101 - APPLIED ELECTRONICS

Date : 09-11-2011 Dept. No. Max. : 100 Marks

Time : 9:00 - 12:00

PART – A

Answer **ALL** the questions (10 X 2 = 20)

1. What is a semiconductor? How is it classified?
2. What is knee voltage?
3. Define CMRR.
4. Calculate the output voltage of a summing amplifier when V_1 = 2V, V_2 = 1V, V_3 = 1.5 V, R_1 = 10 kΩ , R_2 = 10 kΩ , R_3 = 10 kΩ, R_f = 10 kΩ.
5. Simplify Y=$\overline{C}\,\overline{D}$ + $\overline{C}$ D.
6. What is a half subractor?
7. Write a short note on T flip flop.
8. What are shift registers?
9. What is virtual memory?
10. What is hardwired control?

PART – B

Answer any **FOUR** questions (4 X 7.5 =30)

11. Write short notes on (i) LED (ii) solar cell and (iii) Zener diode.
12. Explain the working of a non-inverting amplifier with a neat diagram.
13. Show that NAND is a universal gate.
14. With neat diagram and truth table discuss the working of a 4 bit ring counter.
15. Discuss in detail the computer registers.

PART – C

Answer any **FOUR** questions (4 X 12.5 =50)

16. Describe the operation of a NPN transistor in common emitter mode. Obtain expressions for the input and output characteristics for the same.
17. a. Explain with circuit the working of an Op-amp based 4 bit binary weighted D/A converter. (6.5)

    b. For a 5 bit binary weighted resistor D/A converter determine the analog voltage for inputs (i) 10101 (ii) 11010 and (iii) Full scale voltage. R_f = 1.5R Assume 0 = 0V and 1 = 5V. (6)
18. Simplify using K – map F(A,B,C,D) = Σ (0,3,4,7,8) + Σ_d (10,11,12,13,14,15). Realize the Boolean expression using NAND-NAND network.
19. Explain with circuit the working of clocked RS flip flop. Show the construction of D flip flop using RS flip flop and explain its working.
20. Write short notes on, (a) RAM (b) ROM and (c) cache memory.

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